




Full-Wave Simulation of System-Level Disruption During Secondary ESD Events in a Smartphone

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Abstract—To demonstrate the electromagnetic full-wave simulation of a secondary electrostatic discharge (ESD), an ESD generator is modeled in three dimensions (3D) and in contact mode discharging to a non-grounded, metallic ear-mesh of a smartphone. The nonlinear Rompe–Weizel SPICE model computes the arc resistance of the secondary discharge between ungrounded metal and a grounded enclosure. The SPICE model is solved using a circuit simulator, and the 3-D model is solved using the transmission-line matrix time-domain numerical method. Transient cosimulation is a new technique that is used to solve both circuit and 3-D models at the same time. The simulation predicts the coupling from ESD to a victim trace in the smartphone. Measurements performed at several stages validate the simulation results. Using this novel methodology, the user can simulate the secondary discharge in products to predict ESD damage and disruption on a system level.

Index Terms—Breakdown voltage, cellular phones, circuit simulation, current measurement, electromagnetic coupling, electrostatic discharge (ESD), numerical simulation, spark gaps, time-domain analysis.

I. INTRODUCTION

DISRUPTION and damage from an electrostatic discharge (ESD) can be observed even if the discharge does not directly go into a sensitive trace. An ESD may also cause a secondary ESD event within a product. An example of a secondary ESD is sparking between decorative metal and the grounded housing of a system. Being a function of the capacitance between the decorative metal and the grounded enclosure, the secondary spark currents can reach as high as 600 A—five times higher than that of the primary ESD [1]–[3]; the rise time of this current can be on the order of only a few hundred picoseconds. Two factors contribute to the higher currents and faster rise times. The charged capacitance between the ungrounded metal and the grounded structures forms a low impedance source for the secondary spark. Second, the spark gap is usually a highly overvoltage effect, i.e., the fast charging of the gap by the primary ESD allows the voltage across the secondary gap to reach

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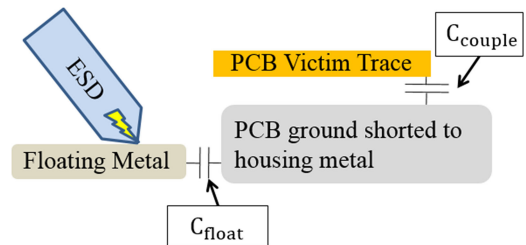


Fig. 1. Illustration of system-level secondary discharge disruption on a victim trace due to capacitive coupling. C_{float} : Capacitance that gets charged between floating metal and metal housing before the breakdown occurs. C_{couple} : Capacitance between PCB trace and PCB ground that causes capacitive coupling.

voltages higher than the static breakdown voltage. So, once the breakdown is initiated, the voltage collapse time will be much shorter than the voltage collapse time of the static breakdown case. Both effects lead to high peak currents associated with sub-nanosecond rise times.

The currents associated with the voltage collapse can couple capacitively and inductively into the circuitry, causing a noise disturbance or even damage [2]. An illustration of the capacitive coupling scenario is shown in Fig. 1.

Techniques for measuring secondary ESD noise on voltage suppressor devices under different operating conditions are described in [3]. There is a need for a simulation methodology to predict the disruption levels for design consideration. Previous works [1] and [4] explain the simulation of the secondary discharge, but do not emphasize the investigation of system-level coupling inside a product. The work presented here uses transient cosimulation to bypass the need for a frequency-domain representation and to make the visualization of transient fields and transient surface currents possible.

II. MODELING OF THE DEVICE UNDER TEST

During the secondary discharge experiment, the ESD generator discharges in a contact mode to the device under test (DUT). The DUT is a smartphone with some details that can be simplified during modeling. The passive model must first be verified before introducing the nonlinear Rompe–Weizel arc model for secondary breakdown. Such validation can be performed by comparing solutions from different solvers or comparing against measurements; for this work, comparisons were made against measured S -parameters. For the verification of

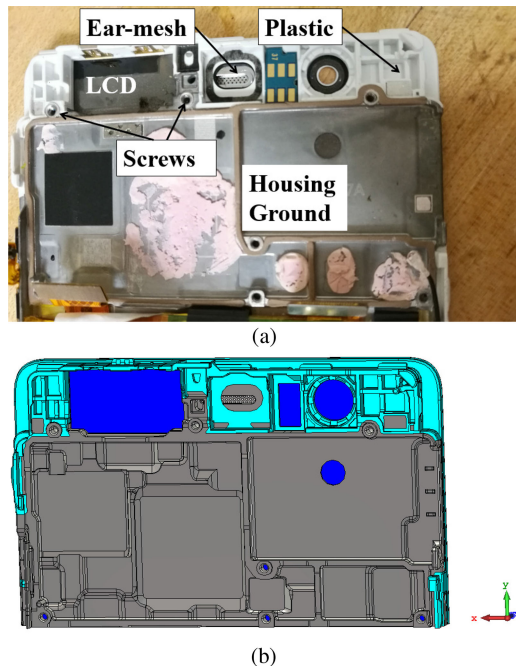


Fig. 2. Back-view of the phone's plastic and metal housing. (a) The real model. (b) The simulation model. The PCB is removed from view, but the floating metal ear-mesh is visible. The ear-mesh, plastic, housing ground, and a few screws are labeled in (a).

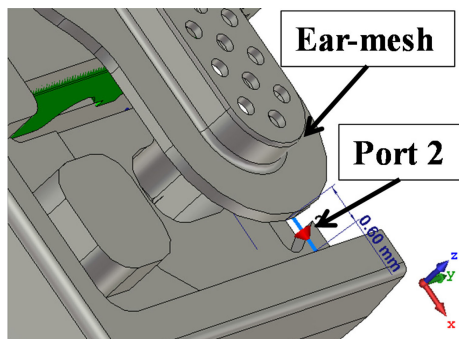


Fig. 3. Spark gap of 0.6 mm between the floating ear-mesh and the smartphone housing ground in the simulation model is shown. S -parameter port 2 is defined at this spark-gap location. The LCD geometry is kept hidden in this view.

the DUT's model, the ESD generator was not modeled, but it was understood that the ESD generator would be in the contact mode to the ear-mesh [see Figs. 2(a) and 3] during the secondary discharge simulation.

A. Description of the Passive Model

S -parameters represent the coupling of a system, so the S -parameters between measurement and simulation are compared to validate the passive model. Port 1 is at the termination of the victim trace (see Fig. 4), while port 2 is between the floating ear-mesh and the housing ground (see Fig. 3).

The charging or discharging of the floating ear-mesh is effectively the input at port 2, and the output of interest is the signal at port 1, so the S -parameter of interest is S_{21} . The phone was kept in the OFF state during the measurements and with

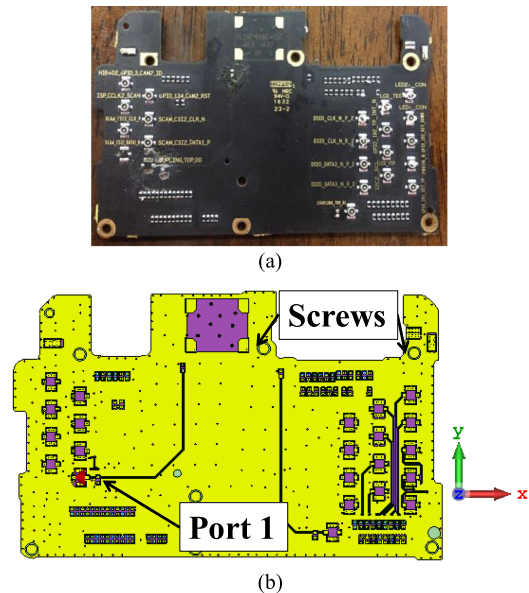


Fig. 4. Main PCB with the victim trace is shown. (a) The real model. (b) The simulation model.

the battery disconnected from the printed circuit board (PCB). The PCB can be removed from the housing, but under testing conditions, the PCB is grounded to the housing via seven screws (see Fig. 4).

B. 3-D Model of the DUT

CST Microwave Studio [5] was used as the modeling tool. Some details in the CAD geometry of the phone and PCB that are not relevant to the modeling of system-level coupling were not considered in the simulation model. The simulation model was restricted to only the top half of the smartphone containing the ear-mesh and the PCB geometry. The white plastic (turquoise in simulation) was modeled as a lossy dielectric. Both the simulation model and the real model are shown in Fig. 2.

The LCD screen (deep blue) was also modeled as a lossy dielectric. With the LCD hidden in Fig. 3, the floating ear-mesh can be seen, and Port 2 is placed at the location of the shortest gap between the ear-mesh and the metal housing ground. This gap distance is 0.6 mm, as shown in Fig. 3. Port 2 is necessary for S -parameter model verification as well as interfacing between the full wave simulator and the SPICE circuit simulator.

The PCB was simplified to include only the top layer containing the victim trace, the closest ground plane, the substrate, the vias, and the solder mask. The PCB imported into CST and the real PCB are depicted in Fig. 4. There are seven screws that connect the housing ground to the PCB ground layers. In CST, they are modeled as cylinders. The trace terminations and the port impedances are all set to 50Ω .

C. Verification of the 3-D Model With Measurement

To verify the three-dimensional (3-D) model, an S -parameter measurement is performed on the real smartphone, as described in Section II-A. Important passives to account for are the



Fig. 5. Audio transducer that sits below the ear-mesh.

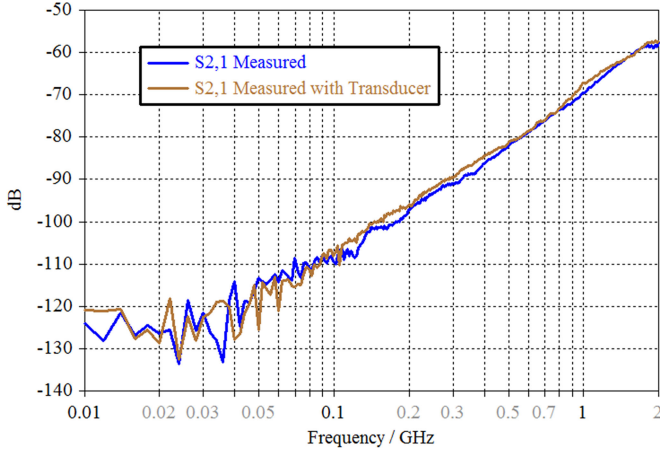


Fig. 6. S -parameter comparison with and without the transducer. Port 2 (see Fig. 3) is between earpiece-mesh and metal housing, and port 1 [see Fig. 4(b)] is between the far end of the victim trace and top layer ground.

metallic structures that can form a capacitive path between the two ports of interest. One such structure is the audio transducer that sits right below the ear-mesh. The transducer is shown in Fig. 5. The effect of the transducer is first tested by performing the same S -parameter comparison with and without the transducer. In Fig. 6, the comparison is shown and it can be concluded that the transducer effect is small enough to not require modeling.

The 3-D model was solved using the transmission-line matrix (TLM) algorithm, which also supports the transient cosimulation that will be used for the secondary discharge simulation. As shown in Fig. 7, there is a good agreement in slope and magnitude when comparing the S -parameters between measurement and simulation. The S_{21} plot shows a 40 dB/dec slope, but a coupling path that is either purely capacitive or purely inductive would result in a 20 dB/dec slope. Since the slope of the S -parameter result is 40 dB/dec, as shown in Fig. 7, the coupling is second order and must include capacitive and inductive coupling. Due to the complexity of the structure, it is not possible to identify the exact structural elements for the inductive coupling path.

The simulation was run with two Tesla K80 GPU cards. The CPU is a 3.4 GHz Intel Xeon E5 v3 processor with 512 GB of DDR4 RAM. The model failed to mesh with the finite element method solver. Since the model had 2 831 782 591 mesh cells, the finite integration technique method could not be used with this hardware. However, the TLM solver was able to lump the mesh cells and reduce the complexity to 6 886 873 mesh cells. The simulation took 65 hours in total for the converged S -parameters.

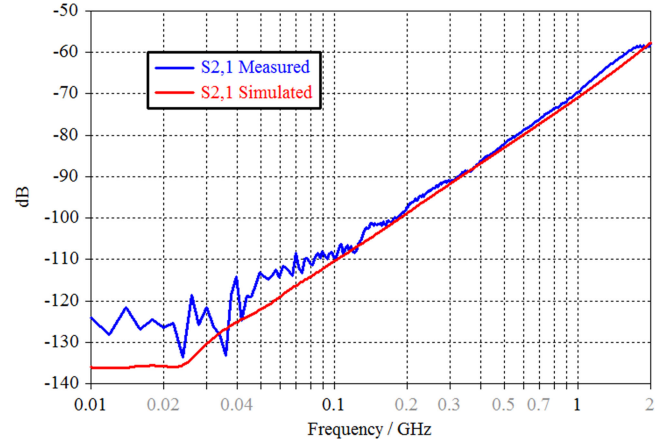


Fig. 7. S -parameter comparison between measurement and simulation of the 3-D smartphone model. Port 2 (see Fig. 3) is between earpiece-mesh and housing metal, and port 1 [see Fig. 4(b)] is between the far end of the victim trace and top layer ground.

III. SECONDARY DISCHARGE SET-UP

A. Physics of the Secondary Discharge Event

For the secondary discharge to occur, floating metal must first be charged relative to the grounded metal [6]–[9]. The test standard requires a contact mode discharge to the floating metal for the model investigated here because the ear-mesh is an exposed conductive surface [10].

Paschen's law governs the breakdown voltage across an air gap [8], [11]–[13]. For homogenous fields, Paschen's voltage is equal to the static breakdown voltage [11], and the breakdown voltage is given as follows [8]:

$$U = 25.4 \cdot d + 6.64\sqrt{d} \quad (1)$$

where d is the gap distance in cm and U is the voltage across the gap in kV.

The voltage in (1) is a necessary but insufficient condition for the breakdown to occur. The movement of the first electron across the gap to begin the breakdown is a stochastic process [14]. The time between when the static breakdown voltage is reached and when the first electron moves through the air gap is called the statistical time lag [15], [16], shown as t_s in Fig. 8. After the first electron moves through the gap, the arc begins to form. From then on, the arc was modeled as a time-varying resistance [11], [12]. Eventually the resistance will collapse, and the time from the formation of the arc to the collapse of its resistance is called the formative time lag [15], [16], shown as t_f in Fig. 8. The model used here for this time-varying resistor representation of the arc is called the Rompe–Weizel model [11]. Its resistance is described as follows:

$$R(t) = \frac{d}{\sqrt{2 \cdot a \cdot \int_0^t i(x)^2 dx}} \quad (2)$$

where R is the arc resistance in Ω , d is the distance of the air gap in meters, a is an empirical constant having a value of $1.0e - 4 \frac{\text{m}^2}{\text{s}}$, and i is the discharge current in amperes.

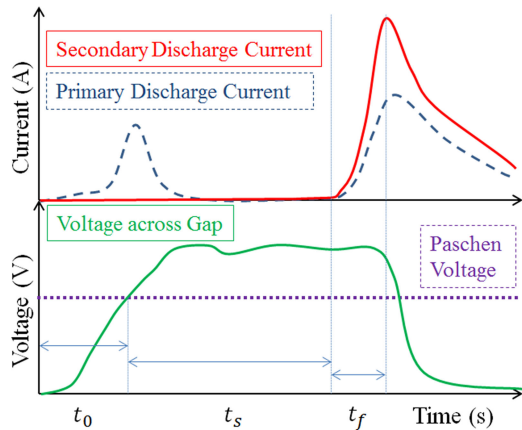


Fig. 8. Illustration of the secondary discharge breakdown process including the voltage across the secondary air gap, an illustration of the secondary discharge current across the air gap, and the primary discharge current charging up the floating metal. Labeled times are t_0 : time to reach Paschen's voltage; t_s : statistical time lag; and t_f : formative time lag.

Fig. 8 illustrates the timing of the secondary discharge process. The overvoltage effect [15], [16] can be seen after t_0 and occurs when the primary ESD excitation uses a voltage much higher than the static breakdown voltage of the secondary gap. During the time period $(t_0 + t_s)$, the local capacitance of the gap between the metal and the ground is charged. After $(t_0 + t_s)$, the charge stored by the local capacitance begins to discharge due to the formation of the arc.

B. Measurement Technique

The measurement technique presented in [17] and [18] was used to perform the detection and monitoring of the secondary ESD. The ESD generator was discharged in the contact mode at the ear-mesh. An F-65 current clamp was used to monitor the primary charging event as well as the secondary ESD. In this geometry, the secondary ESD coupling to victim traces on the main PCB was of interest. A semirigid coax was used for probing the voltage on the critical trace; the semirigid coax ground was well connected to the main PCB ground and ferrites were added to prevent any noise coupling. The secondary ESD event may occur after a primary charging event by a variable time delay, ranging from nanoseconds to milliseconds. To acquire the desired waveforms, an oscilloscope enabled with a fast-retrigger acquisition mode was used, which enabled the capture of multiple ESD events separated by time gaps [17], [18].

Discharge monitoring locations using an F-65 current clamp included the tip of the ESD generator, the ground connection of the DUT, and the ground cable of the ESD generator. The advantage of positioning the F-65 current clamp at the tip of the ESD generator was that position allowed for the capture of high-frequency components of the primary discharge current. By contrast, positioning the F-65 current clamp at the ESD generator ground strap offered the advantage of being convenient in handling, but had the disadvantage of not being able to detect the initial peak current correctly, as shown in Fig. 9.

One limitation of the measurement set-up was that the voltage of the floating ear-mesh could not be measured because the

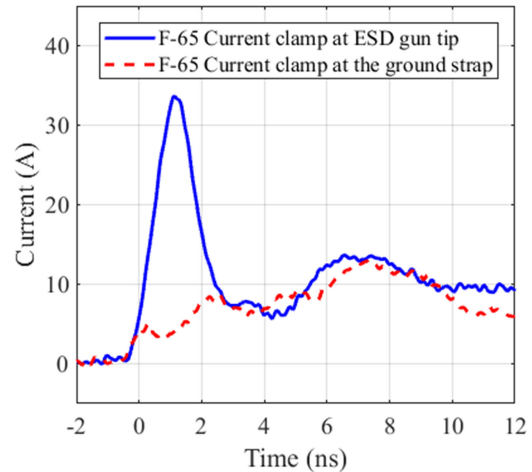


Fig. 9. Comparison of the F-65 current clamp monitor location at the ESD generator tip (blue) and the ESD generator ground strap (red).

voltage probe tip was too large relative to the small ear-mesh; the voltage probe itself would introduce another capacitance and would affect the measurement results.

C. Simulation Set-Up

Transient cosimulation in CST Microwave Studio requires a connection between the ports in the 3-D model and the circuit elements in CST Design Studio [5]. During each time step, voltage and current information is exchanged between the circuit simulator and the full-wave electromagnetic simulator. The TLM algorithm was chosen for the full-wave portion of transient cosimulation [5] since it is the most efficient method for an air-gap discharge in a large computational domain [19]. To prepare the 3-D model of the DUT for secondary discharge simulation, the ESD generator geometry was imported into the DUT's simulation model file. The same ESD generator model was used as in [4] and [19]. The full system is shown in Fig. 10(a), and Port 5 represents the ESD generator relay. As shown in the zoomed view of Fig. 10(b), two more ports, Port 3 and Port 4, were added to the system. Port 3 represents the voltage between the floating ear-mesh and housing ground, while Port 4 represents the contact between the ESD generator tip and the floating ear-mesh. Ports 1 and 2 remained the same as in Figs. 4(b) and 3, respectively.

Fig. 11 shows the connections to the circuit from the 3-D ports. The yellow port 1 in Fig. 11 is used for the 15 kV voltage excitation by the ESD generator. The yellow ports 2, 3, 4, and 5 are termination resistors that have the same values as their respective 3-D ports. For example, yellow Port 3 is connected to a pin labeled "1 (J2305)" and "1" represents the 3-D port number. The secondary discharge current will occur across the 3-D port 2 in Fig. 10(b). The SPICE block for the Rompe–Weizel arc resistance model is described by (2) and the code is given in [11] and [12]. The distance d in (2) is set to 0.6 mm as given in the real structure and shown in Fig. 3. The static breakdown voltage is estimated using Paschen's law at 3150 V. The Rompe–Weizel model alone is not sufficient to create the secondary breakdown process because the secondary breakdown across the gap should

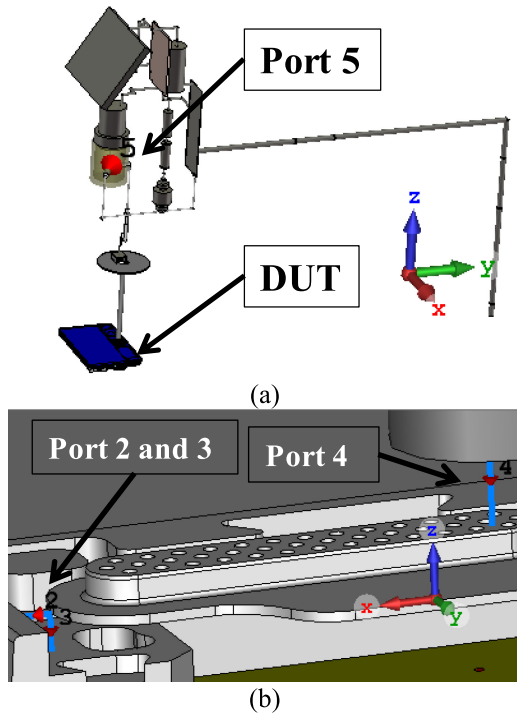


Fig. 10. Secondary discharge 3-D set-up. (a) Full 3-D model with Port 5 and DUT labeled. (b) Zoomed in view of the DUT with the dielectrics hidden and Ports 2, 3, and 4 labeled.

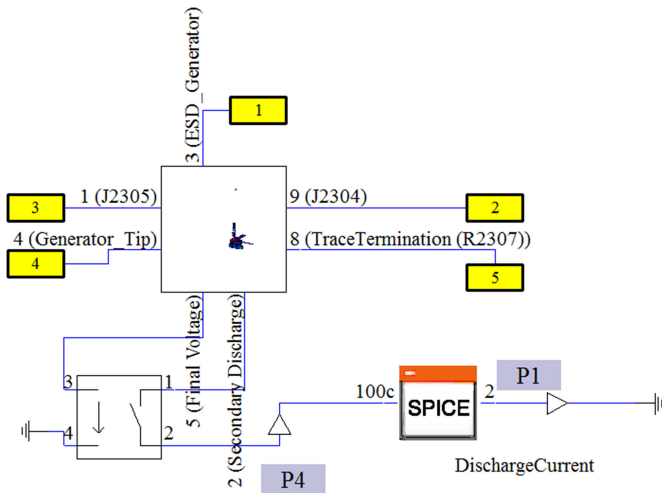


Fig. 11. Secondary discharge schematic showing the connections from the 3-D simulation to the circuit elements.

only occur after the static breakdown voltage is reached. The Rompe–Weizel model alone would incorrectly begin the breakdown at the very start of the simulation. As such, the voltage-controlled switch in Fig. 11 solves this problem by controlling the start of the Rompe–Weizel arc model. The response of the DUT to the secondary discharge depends on the secondary discharge current and rise time. The secondary discharge current depends on the over-voltage across the gap [1], [16]; hence, the voltage-controlled switch is best controlled by the voltage across the gap, which is equivalent to the voltage on Port 3 in

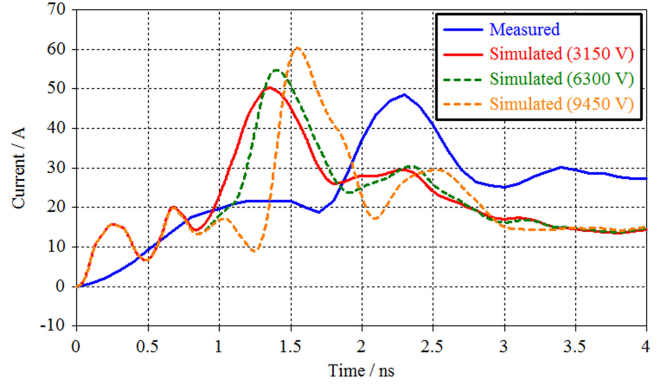


Fig. 12. Comparison of the discharge current waveform at the ESD gun tip in simulation and measurement.

Fig. 10(b). For this experiment, the voltage condition on the voltage-controlled switch was swept for voltages corresponding to Paschen’s voltage, twice Paschen’s voltage, and three times Paschen’s voltage (3150, 6300, and 9450 V, respectively). This provided a range of simulated results, which can be compared to measurements, and this is the proposed workflow for simulations of system-level damage due to secondary ESD.

IV. RESULTS AND ANALYSIS

A. Simulation Prediction and Measurement Comparison

Simulation and measurement results are compared for the cases where the ESD generator is set to 15 kV. Multiple simulations were done with the voltage condition on the voltage switch in Fig. 11 set to be 3150, 6300, and 9450 V.

When comparing the current waveforms in Fig. 12, the peak current value at the ESD generator tip is closest to the simulation result for the voltage switch condition set at 3150 V. From Fig. 12, the formative time lag from the measured current waveform was around 0.7 ns, which is the same as the formative time lag from the simulated current waveform for the 3150 V condition. If a voltage measurement could be performed on the floating ear-mesh relative to the housing ground, then the voltage at which the secondary breakdown occurs could be determined. Without this measurement, the best hypothesis is that the secondary breakdown voltage of the measurement is closer to 3150 V than it is to 6300 V.

In Fig. 13, the voltage waveform on the floating metal during simulation is shown. The arc did not form until the voltage condition was reached. With regards to the formative time lag of the arc, explanation and measurements are given by Fletcher [20]. Fletcher found that the formative time lag does not vary with gap width or the applied voltage—it only varies with the electric field across the gap. Looking at Fig. 13, the simulated result for a voltage condition of 3150 V has around 6000 V across the gap, which corresponds to $\frac{6000 \text{ V}}{0.6 \text{ mm}} = 100 \frac{\text{kV}}{\text{cm}}$ in the gap. Looking up this value for the value of the electric field in the gap from the chart in [20] yields 0.8 ns for the formative time lag, which is close to the measured and simulated results for the 3150 V condition.

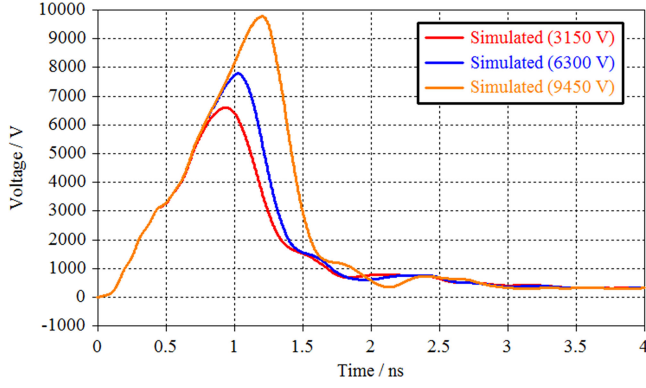


Fig. 13. Simulated voltage waveform on the floating ear-mesh relative to grounded housing.

TABLE I
SIMULATION RESULTS FOR 15 kV ESD GENERATOR SETTING

Voltage condition of switch	Frequency filter	Peak voltage on victim trace	Peak current at ESD generator tip due to the primary discharge	Peak current at ESD generator tip due to the secondary discharge
3150 V	None (60 GHz)	498 mV	19.9 A	50.2 A
	20 GHz	498 mV		
	3 GHz	310 mV		
	2 GHz	238 mV		
	1 GHz	151 mV		
6300 V	None (60 GHz)	858 mV	19.9 A	54.7 A
	20 GHz	848 mV		
	3 GHz	613 mV		
	2 GHz	412 mV		
	1 GHz	218 mV		
9450 V	None (60 GHz)	954 mV	19.9 A	60.3 A
	20 GHz	953 mV		
	3 GHz	784 mV		
	2 GHz	519 mV		
	1 GHz	278 mV		

It is important to understand that in the SPICE representation of (2), there is a setting on the initial condition of the integration value that controls the formation of the arc. The Rompe–Weizel SPICE code in [11] computes the magnitude of the arc resistance with

$$R(t) = \frac{d}{\sqrt{2 \cdot a \cdot V_c(t)}}. \quad (3)$$

Comparing (2) and (3), $\int_0^t i(x)^2 dx$ is numerically equivalent to $V_c(t)$, which is the voltage across a capacitor. The SPICE standard has a variable that the user can set for the initial voltage condition of the capacitor, or $V_c(t = 0)$. If the initial condition is set to be $V_c(t = 0) = 0$ V, then $R(t = 0)$ approaches infinity, no current would flow in any subsequent time steps, and an arc would never occur. Therefore, the initial voltage condition must not be zero, and it will determine the simulation's formative time lag t_f , adding another degree of uncertainty to the simulation. The simulation results are shown in Table I and the measurement results are shown in Table II. For the transient

TABLE II
MEASUREMENT RESULTS FOR 15 kV ESD GENERATOR SETTING

Peak voltage on victim trace	Peak current at ESD generator tip due to the primary discharge	Peak current at ESD generator tip due to the secondary discharge
177 mV	21.5 A	48.8 A

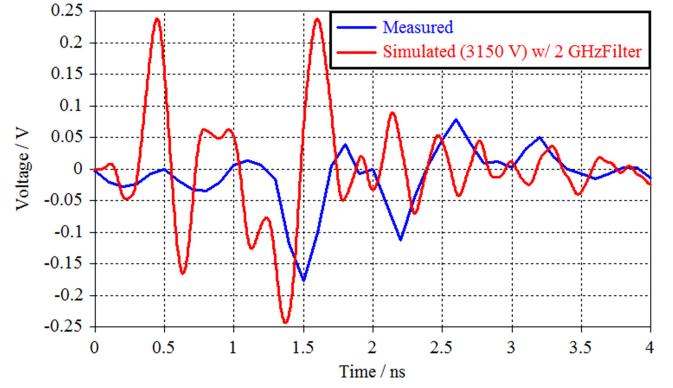


Fig. 14. Voltage waveform induced on the victim trace of interest compared between measurement and simulation. The results are obtained using a secondary gap breakdown voltage of 3150 V and low-pass filtering the simulation results by 2 GHz to match the measurement bandwidth.

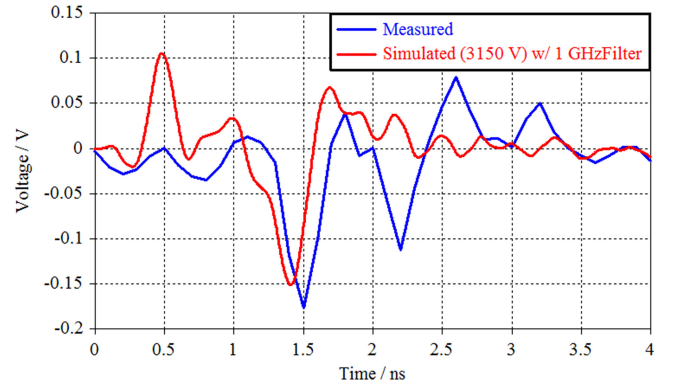


Fig. 15. Voltage waveform induced on the victim trace of interest compared between measurement and simulation. The results are obtained using a secondary gap breakdown voltage of 3150 V and low-pass filtering the simulation results by 1 GHz.

co-simulation, the time sampling rate is 60 GHz. It is known that the oscilloscope used for measuring the induced voltage waveform on the victim trace has a bandwidth limitation of 2 GHz. For this reason, a filter was applied to the simulation results as a postprocessing step to analyze the effect of the frequency limitation of the oscilloscope. Fig. 14 shows the comparison of the simulated voltage waveform filtered to 2 GHz with measurement. Qualitatively, the 2 GHz filtered simulation time signal still showed a much higher frequency ringing than the measurement. Fig. 15 shows the comparison of the simulated voltage waveform filtered to 1 GHz. The simulated voltage waveform filtered to 1 GHz qualitatively matched better in terms of ringing. It is possible that the true measurement bandwidth is between 1 and 2 GHz due to the cables and components in the set-up. Simulation results filtered to 20 GHz showed almost no deviation

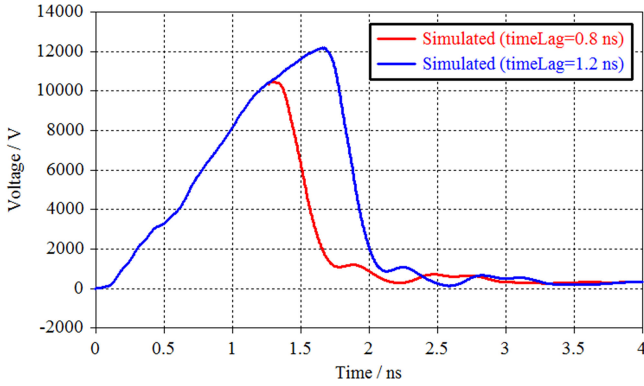


Fig. 16. Voltage waveform on the floating ear-mesh relative to grounded housing. Simulated results with time lag set to be 0.8 and 1.2 ns. Paschen's voltage (3150 V) is reached at 1 ns. ESD generator is set at 15 kV.

from the results without filtering, and so the simulation set-up has a converged sampling rate for the waveforms. Also shown in Table I are results that were filtered to 3 GHz to demonstrate the trend that a narrower frequency band led to lower peak values in the voltage waveform.

Overall, the measured results in Table II fall in the range of predicted values from the simulation in Table I. If the goal is to predict the absolute peak voltage induced on a trace (for example, to make sure that it falls below a certain value to protect an integrated circuit), then the unfiltered peak values should be used to predict the outcome.

Using the same machine with two Tesla K80 GPU cards, the TLM solver was able to lump the mesh cells and reduce the complexity to 8 199 223 mesh cells from 5 326 634 035 mesh cells. The simulation took 272 minutes for a simulation time duration of 4 ns.

B. Time Lag

Time lag is a quantity that is not important from a design perspective [4], but plays an important role in the physics of secondary breakdown. As mentioned in Section III-A, the time lag of the secondary breakdown can be quantified if the voltage across the floating ear-mesh can be measured and the time at which static breakdown voltage is reached can be found. Since this voltage waveform could not be measured for this experiment, as explained in Section III-B, the time lag cannot be computed in this measurement. However, the voltage waveforms are available in simulation, so another set of simulations was done (also at 15 kV ESD generator setting) to show the method of setting the time lag rather than setting the voltage condition.

Fig. 16 shows the voltage between the floating ear-mesh and the grounded housing for statistical time lag settings of 0.8 and 1.2 ns. For these simulations, the voltage-controlled switch in Fig. 11 is replaced with a time-controlled switch that will close after time t_c has been reached in the simulation. Looking at Fig. 16, a gap voltage value that reaches the static breakdown voltage or 3150 V is reached at 1.0 ns, so $t_0 = 1.0$ ns (as defined in Fig. 8). t_c can be set by using

$$t_c = t_0 + t_s. \quad (4)$$

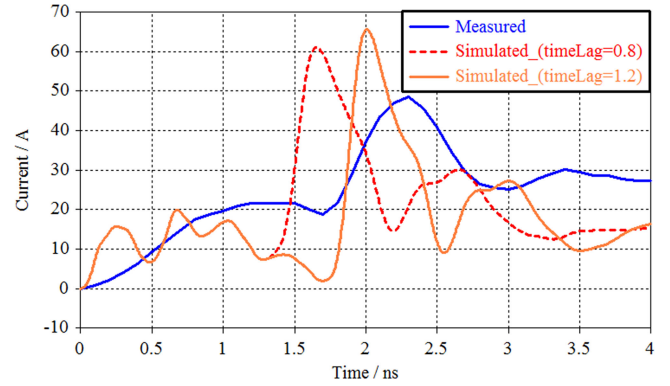


Fig. 17. Discharge current waveform at the ESD generator tip, comparison between measurement and simulations that use the time lag condition.

If the goal is to achieve a statistical time lag of $t_s = 0.8$ ns, then t_c should be set to 1.8 ns. Similarly, for achieving $t_s = 1.2$ ns, t_c should be set to 2.2 ns. For these trials, the simulated current waveforms at the ESD generator tip are shown in Fig. 17. Using the time lag solution path, the peak value of current is higher than the peak value of current using the voltage condition solution path. It is apparent that these t_s values lead to a voltage on the floating ear-mesh that is above 9450 V, and so higher secondary discharge currents and induced voltages on the victim trace are expected.

The level of current from secondary breakdown depends on the conserved quantity, charge (Coulombs), stored across the gap. Though voltage is not a conserved quantity, through the capacitor equation, it is directly proportional to the charge. Hence, the exact value of statistical time lag is not important; only the voltage at which the secondary breakdown occurs matters. Controlling the breakdown condition in simulation using a predefined time lag is not recommended because the time lag parameter does not provide a unique result even in the real world, i.e., the voltage at breakdown can be 5000 V using a time lag of 3 or 10 ns.

V. CONCLUSION

Modeled in 3D was a smartphone susceptible to system level disruption due to secondary breakdown between an ungrounded metal and grounded housing. For the first time, a system-level simulation was performed that could capture noise voltages induced by the secondary ESD. Transient cosimulation was used and did not require computing the entire S -parameter matrix. Two solution paths for controlling the timing of the secondary breakdown in the simulation were given: using a voltage condition and using a time-lag condition. The results were verified by measurements of the noise voltage induced in a victim trace. For future work, the situation of a dual air-gap discharge can be simulated, and the disruption on a system-level can be observed. Instead of the primary discharge being in a contact mode, it would be in a non-contact mode. Two Rompe–Weizel SPICE models would exist in the circuitry, but only the one designated for the secondary discharge would be connected to the voltage-controlled switch.

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